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Stable, Solution-Processed, High-Mobility ZnO Thin-Film Transistors

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Solution-processed thin-film semiconductors can potentially enable low-cost thin-film transistor (TFT) arrays/circuits via mass-manufacturing roll-to-roll processes using a combination of conventional coating and printing techniques (e.g., blade and dip coating, screen and inkjet printing, etc).[1−7] Many soluble organic semiconductors have thus been explored for this purpose, but their functional performances generally fall short of expectation in addition to other process complications. Low mobility, low current density, process-dependent performance variations, and reliability issues are among the critical deficiencies with these materials. On the other hand, inorganic materials such as metal chalcogenides[4−6] have been solution processed into high-mobility thin-film semiconductors, but their inherent toxicity and extreme sensitivities to ambient oxygen and moisture overshadow their performance attributes. Most recently, a thin-film polysilicon semiconductor via thermal decomposition of a solution-deposited silane precursor was reported.[7] High field-effect transistor (FET) mobility reaching ∼6.5 $cm^2\ V^{-1}\ s^{-1}$ and ∼100 $cm^2\ V^{-1}\ s^{-1}$ were achieved for ink-jet printed and spin-coated devices, respectively. However, the attainment of high mobility in this approach relied on a postdeposition laser-induced crystallization of amorphous silicon films generated from thermal decomposition of a silane precursor. Accordingly, this process is essentially similar to conventional polysilicon technology which is still beset with process complications such as uniformity issues.

ZnO is a nontoxic inorganic semiconductor which may also offer such salient features as high mobility, excellent environmental stability, and high transparency. ZnO thin-film semiconductors prepared by radio frequency magnetron sputtering in delicately controlled environments[8] have shown high FET mobility (>30 $cm^2\ V^{-1}\ s^{-1}$), but this technique is not likely to be compatible with low-cost TFT manufacturing processes. In addition, TFTs fabricated by this technique generally failed after several measurements. There were also sporadic studies of solution-processed ZnO thin-film semiconductors for TFTs;[9,10] most however provided FET mobility below 1 $cm^2\ V^{-1}\ s^{-1}$.

We report here our approach to a solution-processed high-mobility ZnO thin-film semiconductor through thermal treatment of a solution fabricated ZnO precursor film at moderate temperatures. By controlling ZnO precursor composition and heating profile, TFTs with a highly oriented polycrystalline ZnO thin-film semiconductor could be obtained, exhibiting FET mobility far exceeding those of amorphous silicon and other similar thin-film semiconductors even when processing and device fabrication/characterization were completely conducted in air. These TFTs demonstrated consistent FET performance and excellent stability under ambient conditions.

In crystalline thin films, ZnO usually adopts a Wurtzite structure with lattice parameters $a = 3.296$ and $c = 5.207$ Å. It is believed that for efficient charge transport in TFTs along the semiconductor channel length, the most favorable ZnO crystal orientation would be one with its (002) plane parallel to or its *c*-axis perpendicular to the substrate.[8] We used a mixture of zinc acetate [$Zn(OAc)_2$] and 2-ethanolamine in methoxyethanol as the precursor and succeeded in achieving a ZnO thin-film semiconductor with this preferential orientation.[11] Thermogravimetric and differential thermal analyses showed that, when heated in air, $Zn(OAc)_2$ began to decompose at ∼190 °C and its thermal decomposition was complete at ∼310 °C (Figure 1a). An exothermic peak appeared between 300 and 400 °C, revealing formation of ZnO crystals. A small exothermic peak between 400 and 500 °C indicated that the crystallization continued, leading to formation of larger crystals. Beyond 500 °C, no detectable weight loss or heat-flow change was observed. These results suggest that an annealing temperature range of 400−500 °C would be most efficient for thermal decomposition of $Zn(OAc)_2$ to crystalline ZnO.

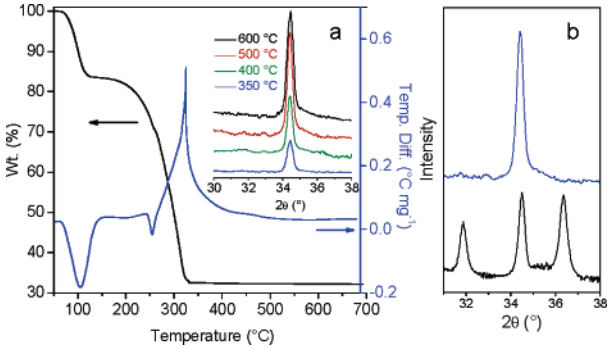

Figure 1. (a) Thermogravimetric analysis and differential thermal analysis of zinc acetate dihydrate at 10 °C min^{-1} ramp rate. The inset shows XRD patterns of ∼40 nm ZnO films on ATO/ITO/glass, showing intensity of (002) peak ($2\theta = 34.4°$) increasing with increased annealing temperature to ∼500 °C, and then leveling off thereafter. (b) XRD patterns of a ZnO film obtained by annealing from 25 to 500 °C at a heating rate ∼10 °C min^{-1}, displaying three distinct peaks at 31.9° (100), 34.4° (002), and 36.3° (101) (black line) and a ZnO film obtained by annealing at 500 °C, showing essentially only (002) peak (blue line).

ZnO thin films on various substrates such as glass, silicon wafer, and ATO/ITO/glass (ATO: aluminum oxide and titanium oxide) were prepared by spin coating a dilute precursor solution of $Zn(OAc)_2$/2-ethanolamine in methoxyethanol, followed by annealing at 300−600 °C. A uniform 40-nm ZnO film could typically be obtained with one to three coatings and annealing at this temperature range. We observed that the heating profile had a decisive impact on the resulting ZnO crystal orientation, thus a profound influence over its FET properties. Specifically, when the ZnO precursor coating was heated gradually from room temperature to 500 °C (∼10 °C min^{-1}) in an oven, the resulting ZnO thin film displayed a rather random crystal orientation in its X-ray diffraction (XRD) pattern where three distinct peaks at 31.8°, 34.4°, and 36.3° representing respectively (100), (002), and (101) ZnO crystal planes were observed (Figure 1b). In sharp contrast, the ZnO thin film

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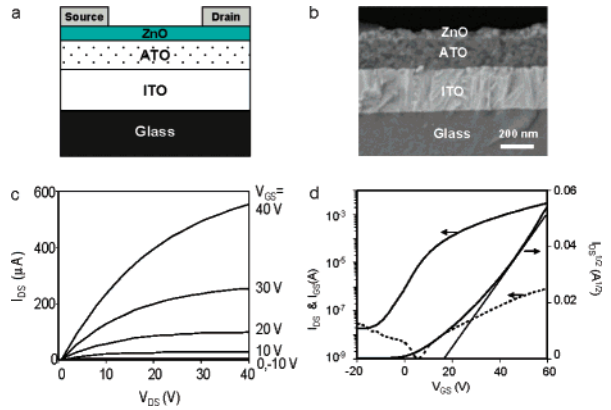

Figure 2. (a) Schematic structure of a TFT device; (b) SEM image of cross-section of a representative TFT test device; (c) plot of drain current, I_{DS}, versus drain voltage, V_{DS}, as a function of gate voltage, V_{GS}, for a TFT test device with a ZnO semiconductor obtained at 500 °C (channel length = 90 μm; channel width = 1000 μm); and (d) corresponding plots of I_{DS} (solid line), $I_{DS}^{-1/2}$, and I_{GS} (dash line) versus V_{GS} at constant V_{DS} = 50 V.

obtained from heating in a preheated oven at 500 °C showed only the (002) peak, demonstrating conclusively a crystalline ZnO thin film with a hexagonal structure and preferred orientation having its *c*-axis perpendicular to the substrate. Applying the full-width at half-maximum of the peak at $2\theta = 34.4°$ to the Scherrer formula gave an average crystal size of ~40 nm for both ZnO crystal films. The scanning electron microscopy (SEM) images of both ZnO films also showed essentially the same smooth surface morphology composing of closely packed particles with a particle size of 30−50 nm (Figure S1, Supporting Information), indicating that each particle was a ZnO single crystal since this particle size was similar to the one calculated from the XRD results.

Bottom-gate, top-contact TFTs were constructed on a ATO/ITO/glass substrate using ATO, ITO, and vacuum deposited thin-film Zn metal, respectively, as gate dielectric, gate electrode, and source/drain electrodes (Figure 2a). Figure 2b shows a SEM image of cross-section of a representative TFT with a 40 nm thick ZnO semiconductor obtained by applying three coatings of $Zn(OAc)_2$/2-ethanolamine/methoxyethanol and annealing at 500 °C. The FET properties of the device fabricated in this manner are shown in Figure 2, parts c and d, which showed *n*-channel behavior operating in accumulation mode on a positive gate bias. The observed FET characteristics conformed closely to the conventional transistor models in both the linear and saturation regimes with I_{DS} increasing linearly with V_{DS} at low drain voltages, and clear saturation behavior at high drain voltages because of pinch-off of the accumulation layer. The extracted saturation mobility and current on-to-off ratio from the transfer plot (Figure 2d) at drain voltage (V_{DS}) of 50 V and gate voltages (V_G) of −20 to 60 V for an unprotected, unpatterned TFT device were 5.25 $cm^2\ V^{-1}\ s^{-1}$ and 1.65×10^5, respectively. The linear mobility was lower with a value of 1.65 $cm^2\ V^{-1}\ s^{-1}$ (V_{DS} = 4 V), which is commonly observed for linear mobility in both organic and inorganic TFTs. In sharp contrast, the device prepared via gradual heating, which resulted in a randomly oriented crystalline ZnO semiconductor, yielded a markedly lower saturation mobility of 0.23 $cm^2\ V^{-1}\ s^{-1}$. This mobility was over an order of magnitude lower and was commonly reported for solution-processed ZnO-TFTs. No visibly distinct differences in surface morphology (see Supporting Information) of these two ZnO semiconductor films could be noted, demonstrating the significance of ZnO crystal orientation on FET behaviors.

The evolution of ZnO crystals in the solution-fabricated precursor thin film as a function of annealing temperature was readily monitored using XRD analysis. Figure 1a (inset) depicts the temperature dependence of XRD traces for ZnO semiconductor thin films, displaying clearly a progressive increase in (002) peak intensity with increasing annealing temperatures up to about 500 °C. This was also reflected in a corresponding increase in the FET mobility of ZnO-TFTs as the annealing temperature was increased to about 500 °C. The extracted saturation mobility for the devices fabricated at 350, 400, 500, and 600 °C were, respectively, 0.40, 2.65, 5.25, and 5.09 $cm^2\ V^{-1}\ s^{-1}$. The fact that the mobility at 600 °C was similar to that at 500 °C indicates that an annealing temperature higher than 500 °C had no effect on device performance. These ZnO-TFTs also exhibited excellent environmental stability. The mobility showed a slight increase during the first 10 days, then leveled off and remained relatively stable thereafter. The initial increase in mobility was attributed to the gradual oxidation of zinc source/drain electrode surface to ZnO surface layer which helped achieve an intimate semiconductor/electrode interfacial contact.

The UV−vis absorption spectrum of a ZnO semiconductor thin film prepared at 500 °C showed a λ_{max} at 363 nm and an optical band gap of 3.31 eV (Figure S3, Supporting Information), which is similar to the value reported for ZnO films.[12] This large band gap was thought to be responsible for the relative insensitivity of ZnO TFTs to ambient light. The I_D-V_{GS} curve measured under a fluorescent lamp was almost the same as that measured in dark. The optical transmittance of the ZnO semiconductor film on a glass substrate was >80% in the spectral range of 400−800 nm, demonstrating excellent transparency.

In conclusion, we have unequivocally demonstrated that the crystal orientation of a ZnO thin-film semiconductor prepared by solution deposition has a profound impact on its FET properties. A highly crystalline ZnO thin-film semiconductor could be prepared via controlled thermal annealing of a solution deposited ZnO coating to give a preferential crystal orientation in which the *c*-axis is normal to the substrate. TFTs incorporating ZnO channel semiconductors of this nature have shown excellent FET characteristics with mobility that is at least an order of magnitude higher than any solution-processed ZnO-TFTs reported to date, thus opening up application opportunities previously contemplated but not realized.

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Supporting Information Available: Instrumentation, details of experimental procedures, and additional figures. This material is available free of charge via the Internet at http://pubs.acs.org.

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